2022 Digital IC Design

Homework 4: Edge-Based Line Average interpolation

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| NAME | | 洪緯宸 | | | | | | |
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| **Simulation Result** | | | | | | | | |
| Functional simulation | Pass | | Gate-level simulation | Pass | Clock  width | 19.4(ns) | Gate-level simulation time | 50040 (ns) |
| your pre-sim result of test patterns | | | | | your post-sim result of test patterns | | | |
| **Synthesis Result** | | | | | | | | |
| Total logic elements | | | | | 258 | | | |
| Total memory bit | | | | | 0 | | | |
| Embedded multiplier 9-bit element | | | | | 0 | | | |
| your flow summary | | | | | | | | |
| **Description of your design** | | | | | | | | |
| 一開始先把奇數排讀出來並同時輸出到memory，再藉由奇數排計算出偶數排，同時輸出到memory，輸出完成把done拉起即完成 | | | | | | | | |

*Scoring = (Total logic elements + total memory bit + 9\*embedded multiplier 9-bit element) (longest gate-level simulation time in ns)*